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(54) Title: CONFIGURABLE MIXED ANALOG AND DIGITAL MODE CONTROLLER SYSTEM

(57) Abstract: A configurable mixed analog and digital mode controller may be fabricated as a single monolithic device such as an integrated circuit semiconductor die or a multi-chip package (MCP). The configurable mixed analog and digital mode controller may be a microcontroller and/or a digital signal processor (DSP) in combination with both analog and digital peripherals that may be configured and connected together, both before and during operation thereof, to function as a complete controller system.

CONFIGURABLE MIXED ANALOG AND DIGITAL MODE CONTROLLER SYSTEM

This patent application is related to commonly owned United States Patent Applications: Serial No. _____, filed _____, entitled "Comparator Programmable for High-Speed or Low-Power Operation" by Hartono Darmawaskita and Miguel Moreno; Serial No. _____, filed _____, entitled "Auto Calibration Circuit to Minimize Input Offset Voltage in an Integrated Circuit Analog Input Device" by Hartono Darmawaskita, Layton Eagar and Miguel Moreno; and Serial No. _____ _____, filed _____, entitled "Input Offset Calibration of an Analog Input Device Using a Microcontroller" by Hartono Darmawaskita, Layton Eagar and Miguel Moreno; these applications are hereby incorporated by reference herein for all purposes.

This invention relates to controller systems having both analog and digital operating parameters, and, more particularly, to a single monolithic device such as an integrated circuit die or multi-chip package comprising a microcontroller and/or a digital signal processor (DSP) in combination with both analog and digital peripherals that may be configured and connected together, both before and during operation thereof, to function as a complete controller system.

Controller systems are becoming more sophisticated while continuing to drop in price. More and more consumer and commercial products, such as for example but not limited to, appliances, telecommunications devices, automobiles, security systems, full-house instant hot water heaters, thermostats, and the like are being operated by these controller systems.

Analog inputs for receiving sensor information and analog outputs for controlling functions are necessary for the application of these controller systems. Heretofore separate and discrete analog interfaces were used to connect a digital controller to the outside world. Digital controllers were created from programmable logic arrays (PLA), field or mask programmable gate arrays (FPGA or PGA), microcontrollers or digital signal processors (DSP) in combination with software or firmware programs.

Analog input devices such as analog-to-digital converters (ADC) in conjunction with a separate operational amplifier were used to convert a time-varying analog signal into digital representations thereof for application to digital inputs of the digital controller and use thereof. Voltage and current levels were also detected by discrete integrated circuit voltage comparators that changed a digital output state when a certain analog value was present on the input of the comparator. Analog control outputs were generated by digital-to-analog converters (DAC) in combination with the digital controller.

Technology has now advanced to the point where the analog input and output devices can be fabricated on the same integrated circuit die or multi-chip package (MCP) as the digital controller, thus producing mixed signal integrated circuits. Mixed signal integrated circuits reduce the cost, size and power consumption of controller systems. A mixed signal controller is described in United States Patent No. 5,821,776, entitled "Field Programmable Gate Array with Mask Programmable Analog Function Circuits" to John E. McGowain. The invention disclosed in this patent uses a field programmable gate array in combination with mask programmed analog functions on an integrated circuit die.

There are a large number of different applications and requirements for control systems, therefore an integrated circuit controller must have a great deal of flexibility and capability for use in various systems configurations. To be cost effective, the integrated circuit controller should be mass-produced as a single monolithic device. Even in a single application, requirements for the integrated circuit controller may change, such as for example, but not limited to, a sleep mode and an operate mode, a low-power mode and a high-speed mode, etc. Analog input peripheral devices of the integrated circuit controller must interface with very different analog input parameters such as speed, gain, offset, common mode rejection, linearity and the like. In addition, different applications may have restrictions on the amount of power available to run the controller and its integral analog peripherals. Since there are so many different combinations of analog input, output and systems parameters, a large number of

different types of integrated circuits having analog and digital capabilities have been required.

What is needed is an integrated circuit controller having both analog and digital capabilities that may be easily configured or programmed for a specific application without special factory setup or testing.

The invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing a configurable mixed analog and digital mode controller fabricated as a single monolithic device such as an integrated circuit semiconductor die or a multi-chip package (MCP). The configurable mixed analog and digital mode controller comprises a processor such as a microcontroller and/or a digital signal processor (DSP) in combination with both analog and digital peripherals that may be configured and connected together, both before and during operation thereof, to function as a complete controller system. Configurable parameter analog devices in combination with an analog switch matrix allows interconnection between the analog devices and connection to input/output (I/O) pads of the integrated circuit die or pins of the MCP. The configurable parameter analog devices and analog switch matrix may be controlled by processor (microcontroller and/or DSP) which is also fabricated on the same integrated circuit die or in the MCP.

In one aspect of the present invention, the processor has, but is not limited to, the following elements/components: program, volatile and non-volatile data storage; general input-output (I/O) ports; general digital peripherals such as timers, UART/USART, I^2C, SPI and the like.

In another aspect of the present invention, digital peripherals may be included to control power devices such as pulse width modulation (PWM) and programmable switched mode controller (PSMC) modules.

In yet another aspect of the present invention, analog peripherals such as digital-to-analog converters (DAC) and operational amplifiers (op-amp) may be included for generating or controlling analog outputs.

In still another aspect of the present invention, analog peripherals such as analog multiplexer switches, op-amps, programmable gain amplifiers (PGA), sample and hold amplifiers, comparators, analog-to-digital converters (ADC), voltage references, analog multipliers and the like may be included and adapted for receiving analog input signals.

A feature of the present invention is programmable gain bandwidth of the analog peripherals.

Still another feature is programmable gain of the analog peripherals.

Another feature is input offset zero calibration of the input offset voltage of the analog peripherals.

Another feature is programmable input offset zero calibration of the input offset voltage of the analog peripherals after every gain bandwidth or gain change of the analog peripherals.

Another feature is turning on and off the analog peripherals so as to conserve system power (sleep mode).

Another feature is access to the inputs and outputs of the analog peripherals to connect feedback components thereto.

Another feature is programmable access to the inputs and outputs of the analog peripherals to connect feedback components thereto.

Another feature is programmable connections between the inputs and outputs of the analog peripherals, and also to input-output pads or pins of the controller package.

Another feature is programmable speed/power for operation of the analog input peripherals such as op-amps and comparators.

Another feature is configuration of a controller interrupt input or status input for connection to a digital output of an analog input voltage comparator.

Another feature is small signal operation at or near a power supply rail voltage.

Another feature is small signal operation at or near ground reference.

Another feature is small signal operation at or near Vcc reference.

It is contemplated and within the scope of the present invention that the configurable mixed analog and digital mode controller may be adapted for configuration depending on the applications or target market for the controller and, may

comprise in combination with the processor (microcontroller and/or DSP), for example, but not limited to:

a) Analog multiplexer switches for enabling analog connections and also input and output analog signal routing to and from the analog peripherals of the controller.

b) An op-amp ahead of an ADC for signal conditioning prior to analog-to-digital conversion, i.e., gain stage, filtering, sensor interface, etc.

c) A programmable gain amplifier (PGA) ahead of the ADC where the combination thereof is adapted for auto ranging applications.

d) A sample and hold amplifier ahead of the ADC, adapted for sampling of one or more analog signals for later ADC conversion. This is especially applicable to power and motor control applications.

e) An op-amp ahead of a comparator for signal conditioning of the signal value to be compared. This enables high resolution firmware assisted analog-to-digital conversion such as delta sigma, slope ADC, etc.

f) An op-amp, comparator and ADC in combination wherein the comparator is adapted for coarse/crude monitoring of analog signal values even during a sleep mode, wherein the ADC may be used for other applications until the comparator detects that a critical event has occurred, requiring the use of the ADC. The ADC can be used for general analog-to-digital conversion, while the op-amp and comparator may be used for higher resolution firmware assisted delta sigma or slope ADC conversion for a selected channel.

g) A comparator in combination with a programmable switched mode controller (PSMC) for creating a complete closed control loop in hardware. The processor need only setup the configuration parameters and set point with minimal firmware overhead and involvement of the processor.

h) An ADC in combination with a DAC or PSMC for creating a complete closed loop control system. The ADC in combination with an op-amp can measure sensor inputs, the processor performs a control algorithm, and the DAC or PSMC interfaces to power actuators.

i) An op-amp in combination with an analog multiplier for use in signal conditioning and signal multiplication in the analog domain, for example, power measurement and metering applications. The op-amp and multiplier combination may also be used for signal modulation and demodulation in communications applications.

j) A programmable gain op-amp in combination with a digital-to-analog converter (DAC) that is connected to one of the inputs of the programmable gain op-amp may be used as an input stage for a low level analog sensor or transducer having a voltage offset. The voltage offset introduced by the sensor may be cancelled out by a voltage of equal value thereto from the DAC to one of the inputs of the op-amp which then combines and cancels out this voltage offset. The low level output from the analog sensor or transducer may be amplified to an optimal voltage level by programming the gain of the programmable gain op-amp. A digital offset value is sent to the input of the DAC from either the processor or from the digital I/O.

In any of the above described combinations and applications thereof, the processor (microcontroller and/or DSP) may also perform other function such as system timing, sequence control, user interface, communications, logging, etc.

The configurable operational amplifier(s), according to the present invention, may comprise, for example, but not limited to, the following programmable features: programmable gain bandwidth product (GBWP), programmable amplifier gain, programmable selection of operational amplifier or comparator modes of operation, input offset zero calibration, ultra low input bias current, rail-to-rail input operation, and rail-to-rail output operation. The configurable op-amp(s) may also be programmed to a "sleep mode" which further reduces system power requirements.

The programmable gain bandwidth product (GBWP) feature enables the configurable op-amp of the invention to be utilized for slow, medium or high speed applications. Conservation of power in battery powered applications is readily facilitated by configuring the op-amp in a low GBWP mode, since the op-amp will consume a minimum amount of power from the power supply (battery).

The programmable gain feature may be utilized for various applications requiring a specific amount of gain. In addition, in combination with an input offset feature, the programmable gain feature may be utilized with sensors requiring both input offset and gain (span) calibration. It is contemplated and within the scope of the embodiments of the present invention that input offset zero calibration of the input offset voltage of the analog peripherals may be performed upon demand and may be programmed to occur whenever a gain change and/or input offset change is made.

The programmable selection of operational amplifier (op-amp) or comparator modes of operation feature enables a configurable op-amp to also be utilized in an application as a comparator in combination with the processor. This feature adds flexibility and increased capabilities in the application of the controller system.

The input offset zero calibration feature may be used to minimize the input offset voltage of the op-amp. This feature enables the op-amp to be used for high gain applications, for example, but not limited to, instrumentation sensors such as temperature, pressure, vibration, humidity, gas, ozone, pH, vibration, battery charge and the like. The input offset zero calibration feature may be invoked on demand during start-up of the controller system or at any time during operation thereof. The input offset zero calibration feature can be performed at different (user programmable/selectable) common-mode input voltage levels. These features enable the op-amp to maintain an extremely low input offset voltage over the entire operating range of voltage and temperature which occurs during operation of the application.

Auto zeroing of the analog input peripherals such as op-amps and programmable gain amplifiers may be easily accomplished by connecting the output to the input of the analog input peripheral, then measuring the output voltage thereof. A voltage offset equal to the measured output voltage may then be used to auto zero the analog input peripheral. This voltage offset may be added or subtracted with a measured input value by calculation in the processor, or the voltage offset may be generated by a digital-to-analog converter whose output is connected to an input of the analog input peripheral.

The ultra low input bias current feature allows the op-amp to be used in very high impedance sensor applications such as, for example but not limited to, smoke detectors, carbon monoxide detectors, chemical sensors, photo detectors and the like.

The rail-to-rail input feature allows the op-amp to be used in applications requiring resolution of small input signal values that are near to one or the other of the power supply rails (such as voltages V_{DD} or V_{SS}).

The rail-to-rail output feature allows the op-amp to take advantage of the entire input range of an analog-to-digital converter (ADC), i.e., maximum use of the total bit range (scale) of the ADC.

It is contemplated and with the scope of the embodiments of the present invention that a plurality of analog devices and digital devices may be fabricated on a single semiconductor integrated circuit die or plurality of dice in a multi-chip package.

Other and further features and advantages will be apparent from the following description of presently preferred embodiments of the invention, given for the purpose of disclosure and taken in conjunction with the accompanying drawings.

Figure 1 is a schematic block diagram of a controller system comprising a processor in combination with integral analog and digital peripherals, and input-output functions on a single semiconductor integrated circuit die or in a multi-chip package (MCP);

Figure 2 is a more detailed schematic block diagram of the analog peripheral and switch portion of the controller system illustrated in Figure 1; and

Figure 3 is a schematic block diagram of digital switches in combination with the embodiment of the controller system of Figure 1.

The invention is a configurable mixed analog and digital mode controller fabricated as a single monolithic device such as an integrated circuit semiconductor die or a multi-chip package (MCP). The configurable mixed analog and digital mode controller comprises a processor, such as a microcontroller and/or a digital signal processor (DSP), in combination with both analog and digital peripherals that may be configured and connected together, both before and during operation thereof, to

function as a complete mixed signal system in a single monolithic integrated circuit package.

Referring now to the drawings, the details of preferred embodiments of the invention are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Figure 1, a schematic block diagram of a controller system comprising a processor in combination with integral analog and digital peripherals, and input-output functions on a single semiconductor integrated circuit die or in a multi-chip package (MCP) is illustrated. The block diagram of Figure 1 is illustrative of a typical controller system on an integrated circuit die or in a MCP and is generally represented by the numeral 100. The controller system 100 comprises a random access memory (RAM) 102, a processor 104, a program memory 106, a non-volatile program memory 132, digital input-output (I/O) 108, a digital-to-analog converter(s) (DAC) 110, an analog multiplier(s) 112, a programmable voltage reference(s) 114, a sample and hold amplifier(s) 116, a programmable gain amplifier(s) (PGA) 118, a programmable switched mode controller (PSMC) 120, analog switches 122, an operational amplifier(s) (op-amp) 124, a comparator(s) 126 and an analog-to-digital converter(s) (ADC) 128. It is contemplated and within the scope of the present invention that more than one of any or all of the aforementioned peripherals may be included in the controller system 100. The processor 104 may control any or all of the aforementioned devices on a data and control bus 130 which may be internal to the integrated circuit die or MCP. The processor 104 may also be coupled to the RAM 102 and program memory 106 on the same or other higher speed memory bus(es). The program memory 106 may be for example, but limited to, electrically programmable read only memory (EPROM), read only memory (ROM), electrically erasable and programmable read only memory (EEPROM/FLASH) and the like. Not illustrated but contemplated and within the scope of the present invention are certain general digital peripherals used in combination with the processor 104. These general digital peripherals may be for example, but not limited to, timers, UART/USART, I^2C, SPI, or

other types of communications peripherals well known to those skilled in the art of digital electronics. The non-volatile data memory may be used, for example but limited to, storing calibration data, device/product identity, etc.

The controller system 100 may be fabricated on one or more integrated circuit dice and enclosed in an integrated circuit package. The integrated circuit package may be, for example, but is not limited to, plastic dual in-line package (PDIP), small outline (SO), shrink small outline package (SSOP), thin shrink small outline package (TSSOP), windowed ceramic dual in-line package (CERDIP), leadless chip carrier (LCC), plastic leaded chip carrier (PLCC), plastic quad flatpack package (PQFP), thin quad flatpack package (TQFP), pin grid array (PGA), ball grid array (BGA), TO-220, T0-247, T0-263 and the like.

Referring to Figure 2, a schematic block diagram of the analog peripheral and switch portion of the controller system of Figure 1 is illustrated. The processor 104 controls the analog switches 122 through a control bus 242. The analog switches 122 may be a switch matrix or any form of switch array known to one of ordinary skill in the art of analog integrated circuits. The analog switches 122 may be used to connect inputs and outputs of the analog peripherals together and/or connect the analog peripherals to analog input-output (I/O) connections of the integrated circuit die or MCP. Signal buses 248 are analog outputs from the analog switch 122 and signal buses 250 are analog inputs to the analog switches 122. Signal bus 246 is a digital output from the processor 104 to the DAC 110. Signal bus 244 is a digital output from the ADC 128 to the processor 104. Control and data information to and from the processor 104 may also be sent on the data and control bus 130 from and to any of the analog peripherals contemplated herein. Signal bus 236 is a digital output from the comparator 126 to, for example, an interrupt or digital input of the processor 104. The PGA 118 may be controlled by the processor over a digital control bus 234 and/or the data and control bus 130 (Figure 1).

Auto zeroing of the analog input peripherals such as op-amps 124 and programmable gain amplifiers 118 may be accomplished, for example, by connecting the output of the op-amp 124 with the bus 250f to the input of the op-amp 124 with the bus 248f, then measuring the output voltage thereof with, for example, the ADC 128

connected with the bus 248h. A voltage offset equal to the measured output voltage may then be used to auto zero the analog input peripheral. This voltage offset may be added or subtracted with a measured input value by calculation in the processor 104, or the voltage offset may be generated by the digital-to-analog converter 110 whose output is connected with the bus 250a to an input of the op-amp 124 with the bus 248f.

The following examples illustrate the flexibility of the present invention. The op-amp 124 may be connected ahead of the ADC 128 by the analog switches 122 connecting bus 250f to bus 248h and bus 248f to bus 240. This allows signal conditioning prior to analog-to-digital conversion, i.e., gain stage, filtering, sensor interface, etc. In addition, feedback components(not illustrated) may also be attached externally through the buses 240 and 238 by means of the analog switches 122.

The PGA 118 may be connected ahead of the ADC 128 by the analog switches 122 connecting bus 250e to bus 248h and bus 248e to bus 240. Thus, the PGA 118 in combination with the processor 104 may be adapted for auto ranging analog input applications.

The sample and hold amplifier 116 may be connected ahead of the ADC 128 by the analog switches 122 connecting bus 250b to bus 248h and bus 248b to bus 240. This combination may be used for sampling one or more analog signals for later ADC conversion. This may be especially advantageous to power and motor control applications.

The op-amp 124 may be connected ahead of the comparator 126 by the analog switches 122 connecting bus 250f to bus 248g and bus 248f to bus 240. This combination allows for signal conditioning of the signal value to be compared, and enables high resolution firmware assisted analog-to-digital conversion such as delta sigma, slope ADC, etc.

The op-amp 124, comparator 126 and ADC 128 are connected in combination by the analog switches 122 connecting bus 240 to bus 248f and bus 250f to bus 248g, and then only connecting bus 248h to bus 250f when needed. This combination enables the comparator to be used for coarse/crude monitoring of analog signal values even during a sleep mode, wherein the ADC 128 may be used for other applications until the

comparator 126 detects that a critical event has occurred on the bus 240, thereby requiring the operation of the ADC 128. The ADC 128 may be used for general analog-to-digital conversion, while the op-amp 124 and comparators 126 may be used for higher resolution firmware assisted (processor 104) delta sigma or slope ADC conversion for a selected channel.

The comparator 126 in combination with the PSMC may be used for creating a fully functional closed control loop in hardware. The processor 104 need only setup the configuration parameters and set point with minimal firmware overhead and involvement. The bus 248g may be connected to bus 240 for an external analog input signal. Referring to Figure 3, the output of the comparator may be connected to an input of the PSMC 120 by digital switches 322 connecting digital bus 350c to bus 348d.

The ADC 128 in combination with either the DAC 110 or PSMC 120 may connected together and adapted for creating a fully functional closed loop control system. The ADC 128 in combination with the op-amp 124 can measure analog sensors (external analog inputs). The processor 104 may perform a control algorithm and the DAC 110 or PSMC 120 may interface to external power actuators (not illustrated).

The op-amp 124 may be used in combination with the analog multiplier 112 for signal conditioning and signal multiplication in the analog domain, for example, power measurement and metering applications. This combination may also be used for signal modulation and demodulation in communications applications. In this aspect of the invention, the input of the op-amp 124 may be connected to the external analog input 240 through the bus 248f, and the output of the op-amp 124 may be connected to the input of the analog multiplier 112 through buses 248d and 250f. Many functional combinations may be utilized in communications circuits and systems by using the analog multiplier 112 as a modulator during transmission of analog information, and as a demodulator during reception of analog information. The analog switches 122 in combination with the processor 104 may easily reconfigure the analog and digital

peripheral interconnections during operation of the control system for a multitude of complex functions performed by a single monolithic integrated circuit die or MCP.

An op-amp 124, having programmable gain, is used in combination with a digital-to-analog converter (DAC) 110 as an input stage for a low level analog sensor (not illustrated) or transducer having an voltage offset. The output of the DAC 110 is connected to one of the inputs of the programmable gain op-amp 124 through buses 250a and 248f. The voltage offset introduced by the sensor may be cancelled out by a voltage of equal value thereto from the DAC 110 to the one of the inputs of the op-amp 124 which then combines and cancels out the offset voltage. A digital offset value is sent to the input of the DAC from the processor 104 through bus 246, or from the digital I/O 108 through buses 350b and 348f.

Referring to Figure 3, a schematic block diagram of digital switches 322 in combination with the controller system of Figure 1 is illustrated. The processor 104 may control digital switches 322 through a control bus 342. The digital switches 322 may be a switch matrix or any form of switch array known to one of ordinary skill in the art of digital integrated circuits. The digital switches 322 may be used to connect digital inputs and outputs of the peripherals together and/or connect the peripherals to the digital input-output (I/O) 108 which is adapted for connections of the integrated circuit die or MCP. Signal buses 348 are digital outputs from the digital switches 322 and signal buses 350 are digital inputs to the digital switches 322. The digital switches 322 in combination with the analog switches 122 allow a very flexible configuration of both the analog and digital peripheral inputs and outputs comprising the control system illustrated in Figure 1. Both internal connections between peripherals and external connections may be easily configured before or during operation of the control system. The configuration flexibility of the present invention makes this integrated circuit device very attractive for high volume, low cost manufacture.

In addition, the low level output from an analog sensor or transducer may be amplified to an optimal voltage level by programming the gain of the programmable gain amplifier 118 over the bus 348g from an external source via the digital I/O 108. The digital outputs of the ADC 128 and/or the digital input of the DAC 110 may be

connected to either internal or external peripherals via the digital switches 322. Whenever the gain of the PGA 118 is changed, input offset zero calibration of the input offset voltage thereof may be performed upon demand and may be programmed to occur whenever the gain change occurs.

The invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the invention has been depicted and described and is defined by reference to particular preferred embodiments of the invention, such references do not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alternation and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts. The depicted and described preferred embodiments of the invention are exemplary only and are not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.

CLAIMS

1. A configurable mixed analog and digital mode controller system, said system comprising:

a processor;

at least one analog peripheral;

at least one digital peripheral;

a plurality of analog switches controlled by said processor; and

a plurality of digital switches controlled by said processor;

wherein said at least one analog peripheral is operationally configured with said plurality of analog switches.

2. The system of claim 1, wherein said processor is a microcontroller.

3. The system of claim 1, wherein said processor is a digital signal processor.

4. The system of claim 1, wherein said processor comprises a microcontroller and a digital signal processor.

5. The system of claim 1, wherein said at least one analog peripheral is selected from the group consisting of a comparator, an operational amplifier, a programmable gain amplifier, an analog multiplier, a programmable voltage reference, a sample and hold amplifier, an analog-to-digital converter and a digital-to-analog converter.

6. The system of claim 5, wherein said at least one digital peripheral is selected from the group consisting of a comparator, a programmable voltage reference, a programmable switched mode controller, digital input-output, timers, UART, USART, I^2C and SPI.

7. The system of claim 1, further comprising circuit functions selected from the group consisting of a random access memory, a program memory, a non-volatile program memory and a serial interface.

8. The system of claim 5, wherein said operational amplifier is connected ahead of said analog-to-digital converter and said operational amplifier is adapted for receiving a signal from an external sensor.

9. The system of claim 5, wherein said operational amplifier is connected ahead of said analog-to-digital converter and said operational amplifier is adapted as a signal filter.

10. The system of claim 6, wherein said programmable gain amplifier is connected ahead of said analog-to-digital converter and in combination with said processor is adapted for auto ranging analog-to-digital conversion.

11. The system of claim 5, wherein said sample and hold amplifier is connected ahead of said analog-to-digital converter and is adapted for sampling of one or more analog signals for subsequent analog-to-digital conversion.

12. The system of claim 5, wherein said operational amplifier is connected ahead of said comparator and is adapted for signal conditioning of a signal value to be compared.

13. The system of claim 5, wherein said operational amplifier, said comparator and said analog-to-digital converter are connected in combination to so that said comparator is adapted for coarse/crude monitoring of analog signal values wherein said analog-to-digital converter may be utilized for other applications until said comparator detects an event requiring use of said analog-to-digital converter.

14. The system of claim 13 wherein said analog-to-digital converter is in a sleep mode until required by detection of the event.

15. The system of claim 13, further comprising said processor in combination with said operational amplifier, said comparator and said analog-to-digital converter wherein said processor assists in high resolution analog-to-digital conversion.

16. The system of claim 6, wherein said comparator and said programmable switched mode controller are connected in combination with said processor and adapted for closed loop control.

17. The system of claim 16, wherein said processor sets up configuration parameters and a set point for the closed loop control.

18. The system of claim 5, wherein said processor, said analog-to-digital converter and said digital-to-analog converter in combination are connected together so as to form a closed loop control system.

19. The system of claim 18, further comprising said operational amplifier connected ahead of said analog-to-digital converter and adapted for measuring sensor inputs.

20. The system of claim 19, wherein said processor performs control algorithms and said digital-to-analog converter is adapted for controlling a power actuator.

21. The system of claim 6, wherein said processor, said analog-to-digital converter and said programmable switched mode controller in combination are connected so as to form a closed loop control system.

22. The system of claim 21, wherein said processor performs control algorithms and said programmable switched mode controller is adapted for controlling a power actuator.

23. The system of claim 5, wherein said operational amplifier and said analog multiplier are configured for conditioning and multiplication of an analog signal.

24. The system of claim 23, wherein said operational amplifier and said analog multiplier are adapted for modulating the analog signal.

25. The system of claim 23, wherein said operational amplifier and said analog multiplier are configured for demodulating the analog signal.

26. The system of claim 6, wherein said processor in combination with said digital peripheral is adapted to perform timing functions, sequence control, user interface, and logging.

27. The system of claim 6, wherein said processor and said analog and digital peripherals are fabricated on an integrated circuit die.

28. The system of claim 27, further comprising an integrated circuit package enclosing said integrated circuit die.

29. The system of claim 28, wherein said integrated circuit package is selected from a group consisting of plastic dual in-line package (PDIP), small outline (SO), shrink small outline package (SSOP), thin shrink small outline package (TSSOP), windowed ceramic dual in-line package (CERDIP), leadless chip carrier (LCC), plastic leaded chip carrier (PLCC), plastic quad flatpack package (PQFP), thin quad flatpack package (TQFP), pin grid array (PGA), ball grid array (BGA), TO-220, T0-247 and T0-263.

30. The system of claim 1, wherein said at least one digital peripheral is operationally configured with said plurality of digital switches.

31. The system of claim 5, wherein said digital-to-analog converter is connected to one input of said operational amplifier and an external sensor is connected to another input of said operational amplifier with said analog switches.

32. The system of claim 31, wherein said digital-to-analog converter supplies an offset voltage to compensate for an offset voltage output of the external sensor.

33. The system of claim 31, wherein said operational amplifier is a programmable gain amplifier programmed to a certain gain for amplifying the external sensor output voltage.

34. The system of claim 5, wherein said programmable voltage reference is programmed by said processor.

35. The system of claim 5, wherein said operational amplifier gain bandwidth is programmed by said processor.

36. The system of claim 5, wherein said digital-to-analog converter is connected to said processor.

37. The system of claim 5, wherein said digital-to-analog converter is connected to said processor.

38. The system of claim 5, wherein power consumption of said operational amplifier is programmable.

39. A configurable mixed analog and digital mode controller system, said system comprising:

a processor;

at least one analog peripheral;

at least one digital peripheral;

a plurality of analog switches controlled by said processor; and

a plurality of digital switches controlled by said processor;

wherein said at least one analog peripheral is auto zeroed with said plurality of analog switches.

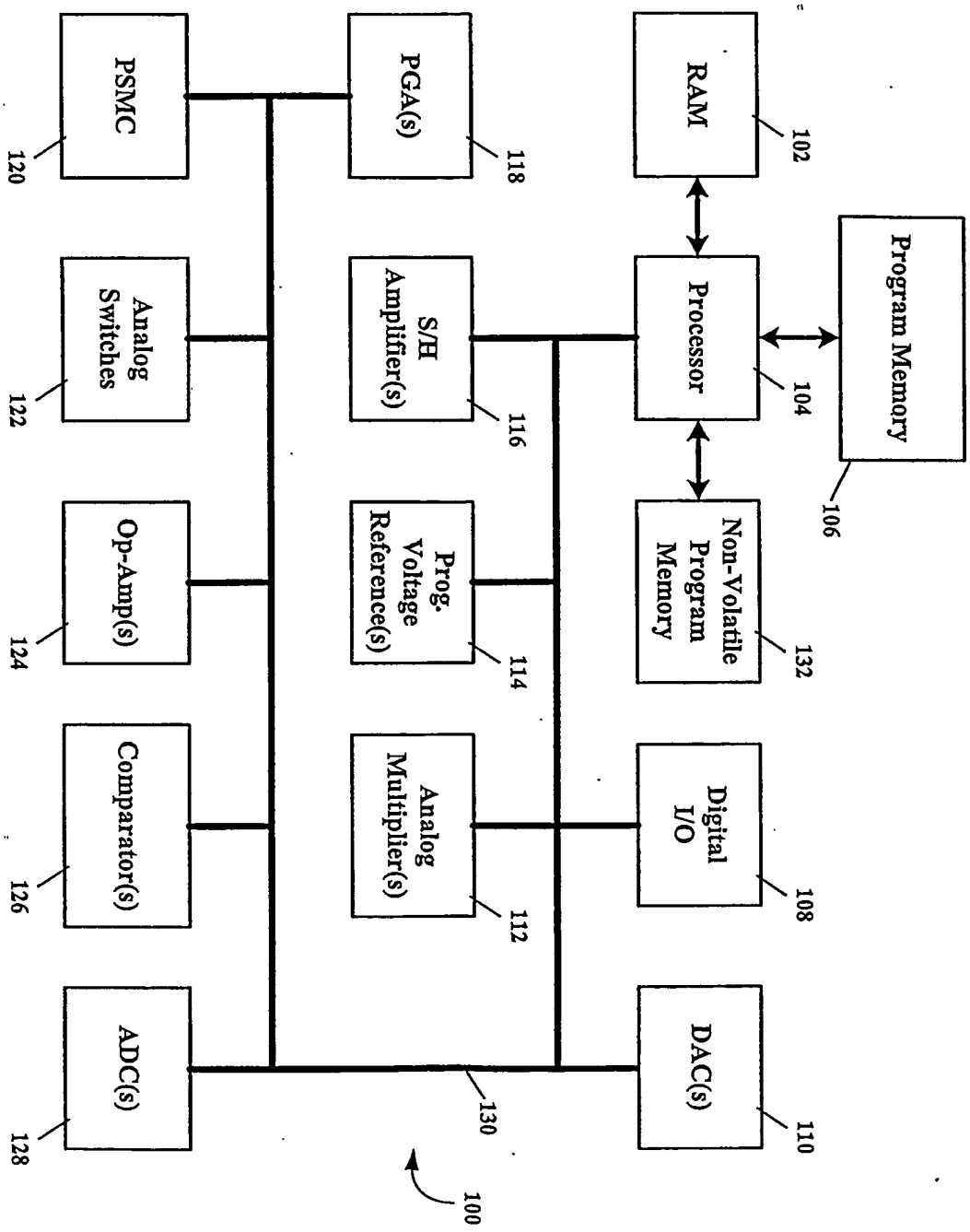
40. The system of claim 39, wherein said at least one analog peripheral input and output are connected together by said plurality of analog switches.

41. The system of claim 40, wherein an output voltage of said at least one analog peripheral is measured.

42. The system of claim 41, wherein the measured output voltage of said at least one analog peripheral is stored in a memory.

43. The system of claim 42, wherein the stored measured output voltage is used to calculate an auto zero offset voltage value.

44. The system of claim 42, wherein the stored measured output voltage is applied to a digital-to-analog converter which is connected to an input of said at least one analog peripheral as an auto zero offset voltage value.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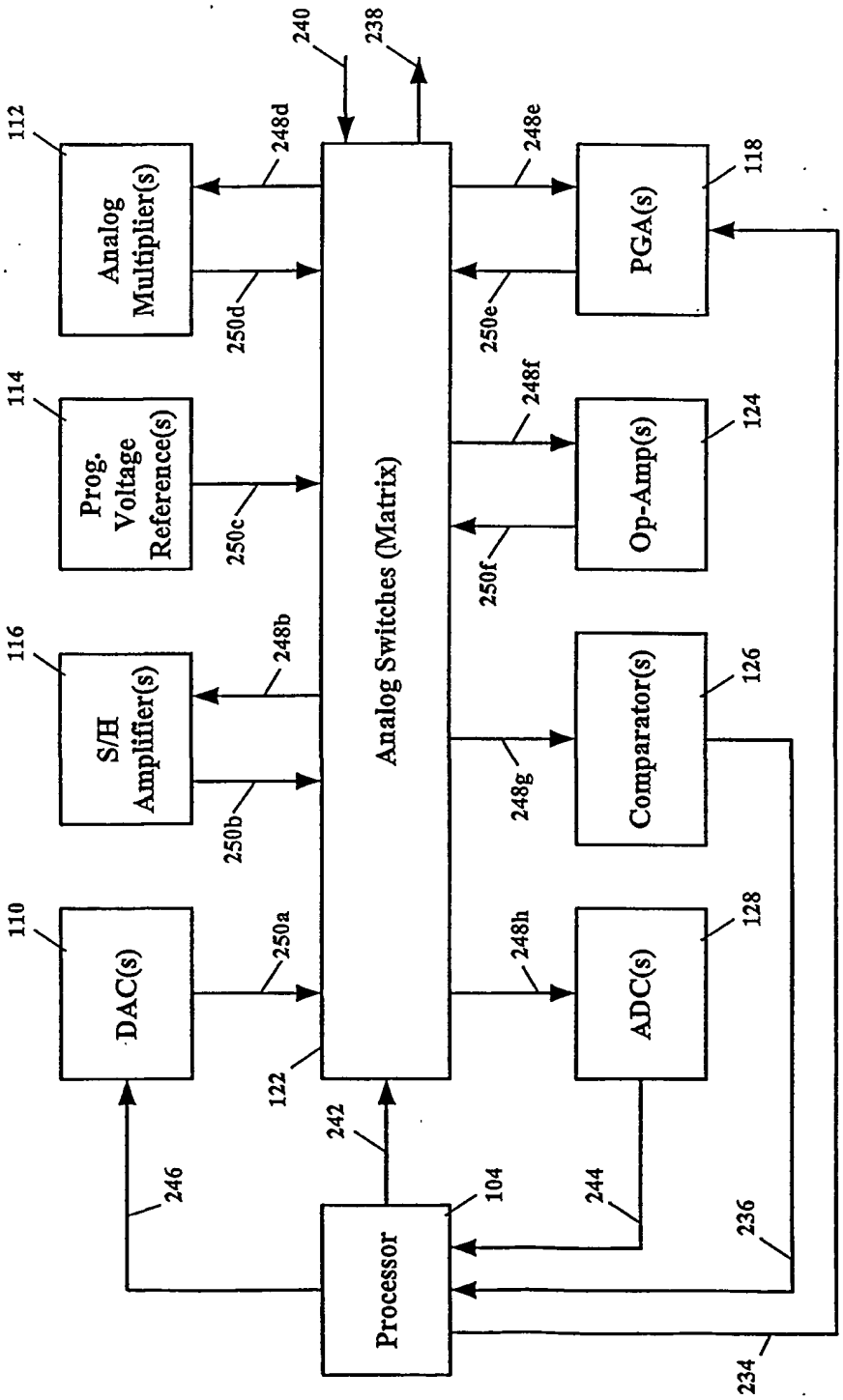
Program Memory
Processor
104
106
PGA(s)
118
PSMC
120
S/H Amplifier(s)
116
Analog Switches
122
Prog. Voltage Reference(s)
114
Op-Amp(s)
124
Non-Volatile Program Memory
132
Analog Multiplier(s)
112
Comparator(s)
126
Digital I/O
108
ADC(s)
128
DAC(s)
110
130
100

FIGURE 1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Prog. Voltage Reference(s)
S/H Amplifier(s)
DAC(s)
Analog Switches (Matrix)
PGA(s)
Op-Amp(s)
Comparator(s)
ADC(s)
Processor
112
114
116
110
122
118
124
126
128
104
240
238
248d
248e
248f
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248h
250d
250e
250f
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250b
250a
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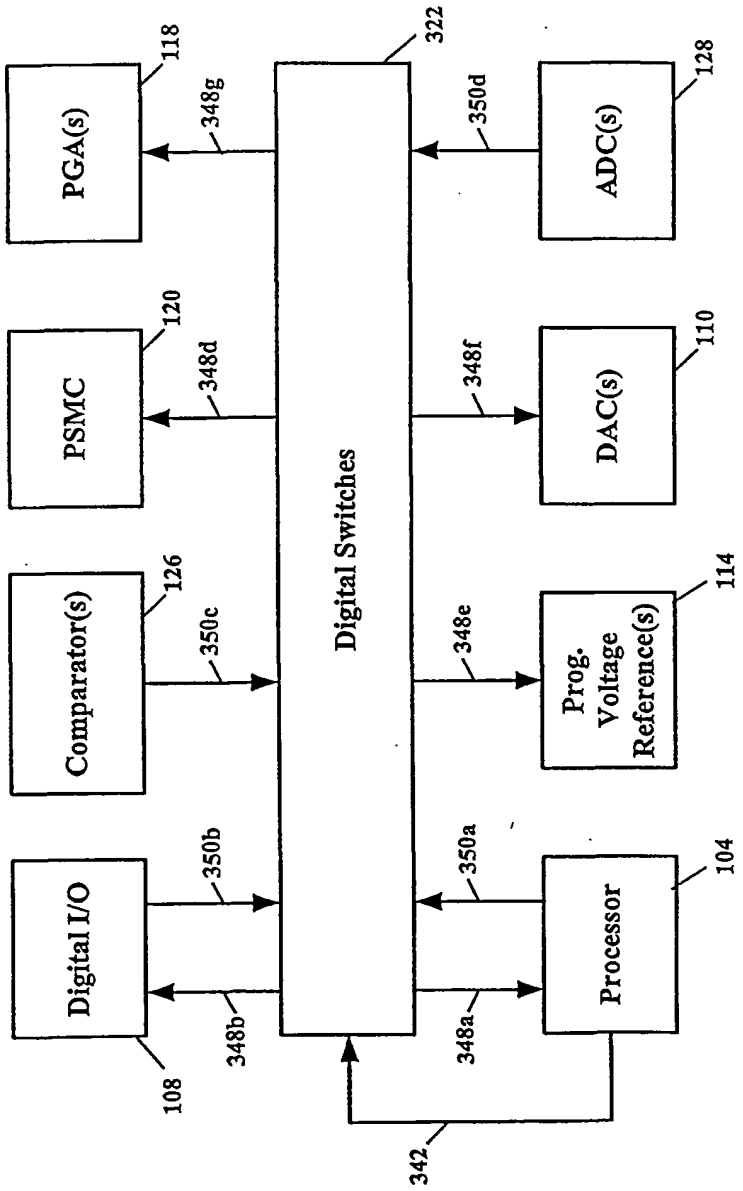
236
234

FIGURE 2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118
348g
Digital Switches
322
350d
ADC(s)
128
PSMC
120
348d
348f
DAC(s)
110
Comparator(s)
126
350c
348e
Prog. Voltage Reference(s)
114
Digital I/O
350b
350a
Processor
104
108
348b
348a
342

FIGURE 3